

Evaluation of Integrated Electrodes for Electrical Capacitance Tomography

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Abstract – Noise immunity in the charge-discharge circuit, which has proved very effective for electrical capacitance tomography, is improved by increasing the clock frequency which, as a result, increases the gain of the circuit. This frequency is limited by the stray capacitance which is largely due to the connecting wires. The present paper describes a system which eliminates the coaxial wires by mounting the circuitry directly onto the electrodes. This is achieved by implementing as much of the circuitry as possible on a custom integrated circuit.

Twelve “integrated electrodes” have been fabricated. These have been tested on a 10 cm diameter plastic pipe. Using 1 metre of coaxial cable the sensors exhibit a worst case signal to noise ratio of 48dB. When the circuitry is mounted directly onto the electrodes this is increased to 58dB. This is the first implementation of an electrical capacitance tomogram, using the charge-discharge circuit, that is based entirely on CMOS technology.

Keywords: electrical capacitance tomography, custom IC, stray capacitance

1. INTRODUCTION

The first practical electrical capacitance tomography (ECT) system was based upon the charge-discharge circuit [1] as shown in Figure 1.

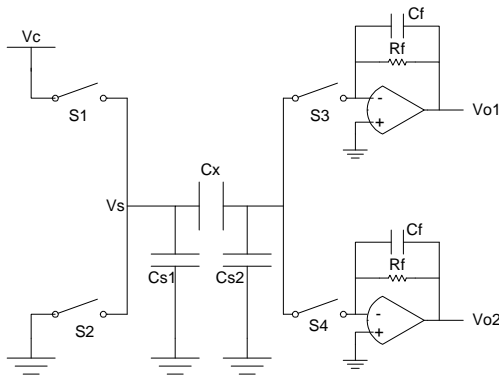


Figure 1 - Charge-Discharge Circuit

The remainder of this section presents an analysis of this circuit to demonstrate why the stray capacitance C_{s1} determines the overall signal to noise ratio (SNR) of the measurements. Section 2 explains how an integrated charge-discharge circuit can overcome the stray capacitance and then describes the architecture of the resulting system. Section 3 presents results from measurements using the integrated electrodes when they are mounted directly onto a small plastic pipe.

1.1 Charge-Discharge Circuit

From earlier work the differential output of the sensor (V_{dif}) has been shown to be [2]

$$V_{dif} = V_{o1} - V_{o2} = 2 C_x V_c f_s R_f \quad (1)$$

where C_x is the unknown capacitance, V_c the magnitude of the source, f_s the source frequency and R_f is the feedback resistor. Clearly the circuit is useful for measuring capacitance as the output is directly proportional to C_x .

An important issue with instrumentation design is the performance of the circuit in the presence of noise, which is generated by external interference and thermal effects within components. Careful design can limit but not remove this noise, so the bandwidth of the system is reduced to reject as much as possible.

The feedback capacitor C_f determines the bandwidth of the sensor, as the dominate pole (f_p) of the circuit is given by [3]:

$$f_p = 1/2\pi R_f C_f \quad (2)$$

To achieve 12-bit resolution the circuit must be left to settle to within 0.01% of its final value before the output is sampled. It can be shown that the settling time (T_s) is given by :

$$T_s = 9/f_p = 18\pi R_f C_f \quad (3)$$

Clearly the settling time increases with C_f while the bandwidth decreases. Hence improvements in the SNR of the output, by limiting the bandwidth, will be obtained at the expense of reducing the measurement rate (increasing the settling time). The desired measurement rate of a tomographic system is determined by the dynamics of the process that is being imaged. The feedback capacitor, C_f , must reduce the bandwidth, without compromising the measurement rate. Consequently the noise level of the charge-discharge circuit is fixed and the only way to improve the SNR is to maximise V_{dif} in Equation 1 without affecting the settling time given by Equation 3. The maximum allowed value of V_c is, essentially, determined by the power supply and therefore, to improve the SNR, the clock frequency, f_s , must be increased.

Now consider the stray capacitance. C_{s2} lies between ground and a virtual earth so its effect on the circuit will be negligible. Let V_s be the actual voltage on the source electrode, so Equation 1 should be:

$$V_{dif} = 2 C_x V_{smax} f_s R_f \quad (4)$$

where V_{smax} is the maximum value achieved by V_s .

S1 and S2 will switch V_s between V_c and ground, which in turn will cause C_{s1} to charge between V_c and ground. The rising edge of V_s will thus be an exponential charge curve where R_s is the resistance of the CMOS switch:

$$V_s(t) = V_c (1 - e^{-t/R_s C_{s1}}) \quad (5)$$

If the switching frequency is f_s then the maximum value of V_s (V_{smax}) is:

$$V_{smax} = V_c (1 - e^{-1/f_s R_s C_{s1}}) \quad (6)$$

Equation 4 suggests that f_s should be as large as possible, but equation 6 indicates that as f_s increases V_{smax} and therefore V_{dif} decreases exponentially. This means that at high frequencies the loss in gain due to the reduction in V_{smax} will outweigh the increase in gain due to f_s , as demonstrated in Figure 2.

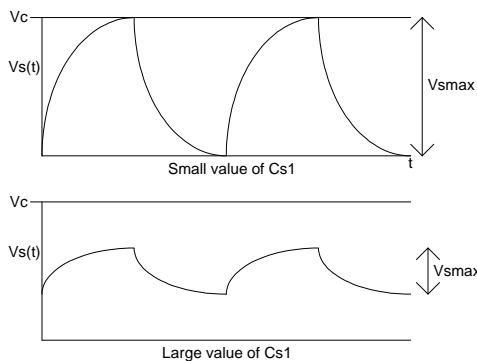


Figure 2 - effect of stray capacitance on source voltage

Therefore equation 6 places a limit on the maximum possible signal level, which in turn limits the SNR.

To reduce the effect of Equation 6 on Equation 4 the exponential term has to be as small as possible:

$$\begin{aligned} 1/f_s R_s C_{s1} &\rightarrow \infty \\ f_s R_s C_{s1} &\rightarrow 0 \end{aligned} \quad (7)$$

The resistance of the CMOS switches (R_s) is approximately 50Ω which is a small value that is difficult to reduce further, therefore the aim is to reduce the stray capacitance (C_{s1}) due to the electrode connection. The value of C_{s1} is directly related to the length of the coaxial cable which should be reduced as much as possible in order to maximise the SNR.

2. IMPLEMENTATION

It is clear from the preceding analysis that there is a need to reduce the stray capacitance to maximise the SNR of the measurements. The minimum stray can be achieved by mounting the sensor electronics directly to the electrode. To do this effectively the electronics have to be physically small, which can be best achieved through integration.

Each Integrated Electrode (IE) will have the ability to be a charge-discharge source or detector, so during operation one will be a source and the other 11 detectors. A pipe containing a perspex phantom of relative permittivity 2.6 will have a maximum standing capacitance of 1pF [1], so the output from the charge-discharge circuit has to be offset to normalise the measurement. The adjacent electrodes will exhibit a capacitance change in the order of 0.1pF while opposite will experience changes of about 0.01pF [1]. A programmable gain will be required to cope with this large dynamic range.

Previous implementations of the charge-discharge circuit [1] have used a 12-bit Analogue to Digital Converter (ADC) to digitise the measurements and a 16-bit Digital to Analogue Converter (DAC) to provide the offset. It is uneconomical to place converters of this resolution onto an integrated circuit. This is because a N-bit converter requires components with tolerances better than $100\%/2^N$. Resolutions better than 10-bit can only be achieved by laser trimming features on the chip, which is extremely expensive for low volume production. The IEs will use off-chip ADCs and DACs to demonstrate the principle and determine what resolution is actually required, but if mass-produced it would be possible to integrate everything onto the device.

The sensors require a digital interface to receive control information and return digital measurements. To ensure easy assembly it is important to minimise the number of interface connections without compromising the frame rate. It will be shown that this can be achieved with a serial "daisy chain." A "controller" will then interface the IEs to a PC.

An integrated circuit, implemented using $0.8\mu\text{m}$ CMOS technology, has been designed and manufactured to act as the front end sensor for ECT. This section describes the architecture of this device which has been described in more detail in [4].

2.1 Analogue Circuit

The analogue circuit within each integrated electrode (IE) is shown in Figure 3.

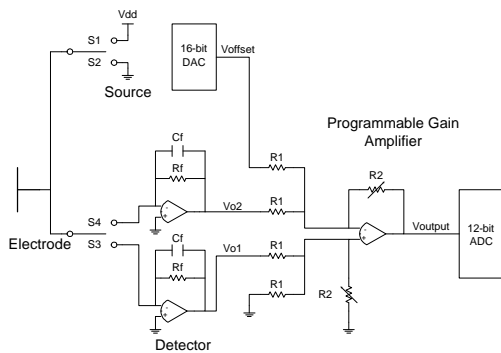


Figure 3 - Analogue Circuit

Each IE contains a charge-discharge source and detector. The clocks that are supplied to S1, S2, S3 and S4 are configured to determine the role of each sensor.

To normalise the capacitance measurements it is necessary to subtract an offset and to employ a variable gain [1]. This is achieved using the differential amplifier that is associated with the programmable gain amplifier. The output of the programmable gain/offset circuit, V_{output} is given by :

$$V_{\text{output}} = K((V_{o1} - V_{o2}) - V_{\text{offset}}) = K(V_{\text{diff}} - V_{\text{offset}}) \tag{8}$$

V_{offset} subtracts from V_{diff} (as defined in section 1) to compensate for the standing capacitance. If R1 and R2 are the op-amp feedback resistors, then K is equal to:

$$K = R2 / R1 \tag{9}$$

R2 is a digitally programmable resistor of value, 200R1, 180R1, 160R1, ..., 60R1, 40R1, 20R1, therefore K can be programmed to have the discrete values 200, 180, ..., 40, 20. The maximum normalised output $\Delta Cx=0.1\text{pF}$ is 20 times smaller than the maximum value of $Cx=2\text{pF}$, and the change in capacitance associated with adjacent electrodes is 10 times greater than that for opposite electrodes [1], so the available values of K ensure a full scale deflection for both adjacent and opposite electrodes.

The whole of the analogue circuit contains only 3 op-amps, as opposed to the 5 amplifiers used within the discrete version [1]. Reducing the number of components will minimise the thermal noise generated in the circuit.

Therefore V_{output} will be a normalised analogue value that is proportional to the maximum change in capacitance. This then feeds into the ADC to generate a normalised digital measurement. V_{offset} is generated digitally with the DAC.

It will be shown in section 3 that the SNR of the integrated electrodes is 58dB, which is equivalent to 10-bit resolution and therefore a 12-bit ADC is appropriate for digitising the output. The gain of the system can vary by a factor of 10 and therefore it is necessary to make the offset 10 times more precise. Therefore a 16-bit DAC is required to generate V_{offset} .

2.2 Digital Circuit

Before a measurement can be taken each electrode is supplied with a 1-bit instruction, to configure the IE as either a source or a detector, a 4-bit gain, from 1 to 10, and a 16-bit offset, giving a total of 21 bits. After the settling time has elapsed a 12-bit measurement has to be returned to the controller. A digital interface, as shown in Figure 4, is used to connect the 12 IEs together. This provides good noise immunity and, by employing a bit-serial strategy, reduces the number of wires. A single clock synchronises the operation of all the integrated electrodes.

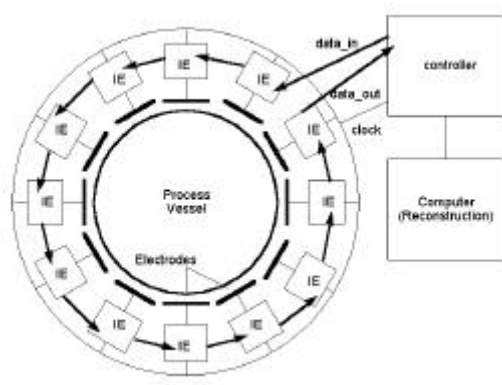


Figure 4 - Serial daisy chain

As each IE requires 21 bits to configure it before a measurement, then 12 electrodes require 252 bits. Similarly, after the 12 bit measurement has been made, 144 measurement bits will be returned. If a serial link is used then while the 252 configuration bits are being supplied to the IE via "data in" the measurement bits from the previous measurement are transmitted from the IE via "data out". After $100\mu\text{s}$, which is the normal settling time of the charge-discharge circuit [1], a maximum of 252 bits has to be transmitted serially, which implies a bit rate of 2.5 Mbits/s.

The IEs have three external digital connections, data in, data out and a clock. The clock is at 10MHz to make the digital logic faster than the daisy chain, and then stepped down to produce the maximum possible charge-discharge clock within the limitations imposed by the stray capacitance [1].

A complete frame of measurements requires 11 electrodes to act as a source [1]. With a $100\mu\text{s}$ settling time, the total measurement time will be 1.1ms which is 909 measurement frames per second. This is significantly faster than existing discrete component systems which have a typical speed of 100 frames per second [1].

The digital logic to implement the serial interface and the digital control for the analogue circuitry has been implemented on the IE and with a Field Programmable Logic Device (FPGA). The FPGA can be reconfigured to allow the functionality of the system to be altered at a latter date.

3. RESULTS

The integrated electrodes have been assembled around a 10cm diameter plastic pipe as shown in Figure 5.

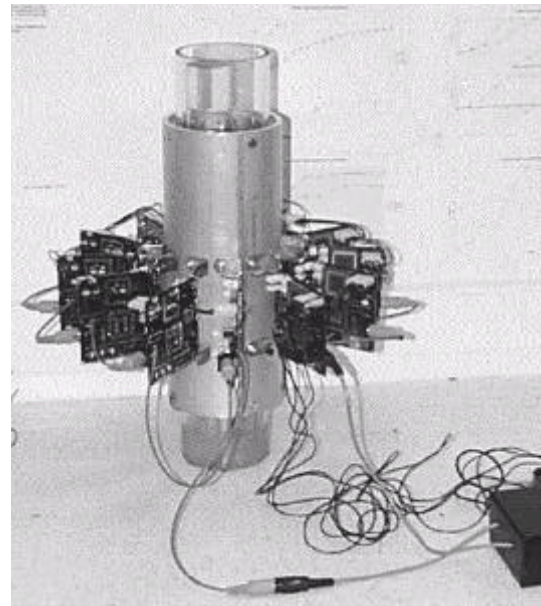


Figure 5 - IE ECT System

Initially all 12 IEs were connected to the electrodes via a 1m length of coaxial cable each having an effective stray capacitance of approximately 100pF. In this configuration the maximum source frequency that caused no loss in gain was found to be 385kHz. The system was calibrated, then filled with the material of maximum permittivity. Ten measurements were made in quick succession which resulted in an average normalised measurement of 3967 with a difference of 16 between the minimum and maximum measurement. This give a SNR of:

$$20 \log (3967/16) = 48\text{dB}$$

which over a full scale of 0.1pF equates to a precision of:

$$(0.1\text{p} \times 16)/3967 = 0.398\text{fF}$$

When the IE circuitry was mounted directly onto the electrodes, as shown in Figure 5, it was possible to increase the clock frequency to 833kHz to give an average over ten measurement of 3279 with maximum variation of 4. This is a SNR of 58dB and a precision of 0.126fF, which demonstrates the advantage of directly mounting the electronics onto the electrodes.

The outputs from the IEs is very closely matched. This is because the gain is set by external components with 1% tolerance so the variation in gain between IEs will be less than 1%. The main difference is the DC offset, which varied by up to 5% between electrodes. In practice this is not a problem as it can be compensated for using the offset.

The DC offset of the circuit is also temperature dependent, so the electronics must be left to reach a stable temperature before use. The system was left for 2 hours then calibrated. It was then switched off for 1 hour then switched back on again. After calibration the output from an empty pipe should be zero, but the actual output over time can be seen in Figure 6.

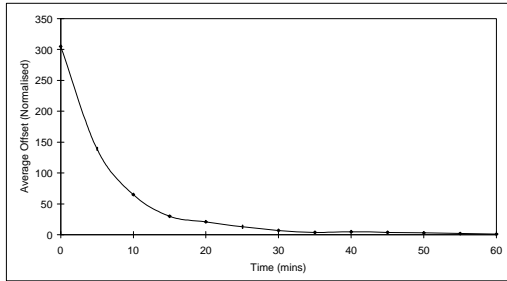


Figure 6 - Variation of Offset with Time

This shows that after 30 minutes the DC offset has reduced to normal levels, so to ensure accuracy the IEs must be left for this time before use.

Figure 7 shows a plot of digital normalised output against C_x for adjacent electrodes (best case) and Figure 8 gives the same information for opposite electrodes (worse case).

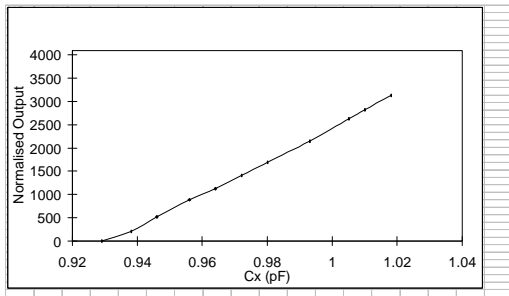


Figure 7- Response from Adjacent Electrodes

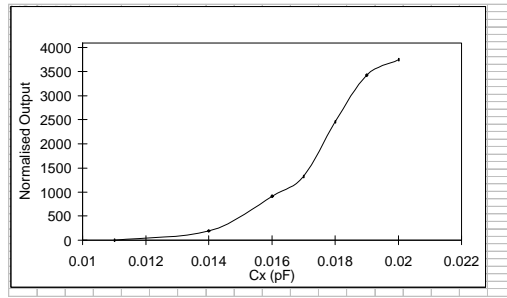


Figure 8 - Response from Opposite Electrodes

The value of the unknown capacitance C_x in the above graphs was measured using a commercial impedance analyser. This was only able to measure accurately down to 1fF, which explains the non-linearity in the graphs. Even though the outputs from the IEs were stable the output from the impedance analyser varied considerably making it impossible to verify the values of C_x for opposite electrodes.

It can be seen from these graphs that the IEs are capable of measuring C_x over the capacitance range observed around a laboratory scale vessel. These results are identical to "spice" simulations of the analog circuit performed while designing the IEs [2].

The final step was to reconstruct images using the linear back projection algorithm. Firstly the circuitry was mounted directly on a set of electrodes that were placed around a 10 cm diameter plastic pipe. Plastic rods were placed in the pipe and images produced off-line, as shown in the left hand images in Figure 9. The measurements were then repeated with the same phantoms, but this time the circuitry was connected to the electrodes via 1m of coaxial cable. Representative results are shown in the right hand images in Figure 9.

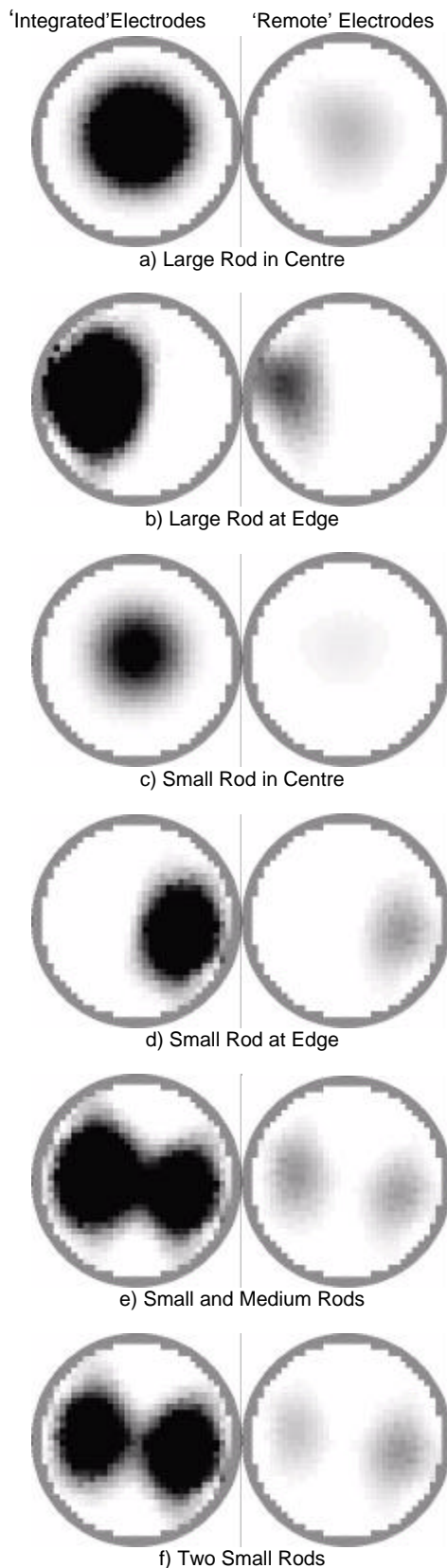


Figure 9 : Reconstructed Images

The left hand images, from the 'integrated' electrodes are clearly superior. It should be noted that the actual diameters of the large, medium and small rods are, respectively, 50%, 40% and 30% of the internal diameter of the pipe.

4. DISCUSSION & SUMMARY

It has been shown that the main factor limiting the SNR of the charge-discharge circuit is the stray capacitance between the electrode connection and ground. This limitation can be overcome by mounting the electronics directly onto the electrode. Measurements have revealed an increase in SNR from 48dB to 58dB when the circuitry is mounted directly on the electrodes, which equates to an improvement in precision from 0.398fF to 0.126fF. This in turn leads to an improvement in reconstructed image quality.

Direct mounting would be difficult with a conventional discrete component implementation due to the physical size of such an arrangement. The solution has been to integrate parts of the analogue and digital electronics onto a full custom chip.

It has also been necessary to design a digital interface to connect the integrated electrodes together, because each of the 12 IEs requires control information and must return digital capacitance measurements. If the IEs are to be easy to assemble the digital interface must contain the minimum number of wires. By using a serial "daisy chain" it is possible to interface the IEs with only 3 wires plus power supply.

The result of this work is an integrated sensor front end capable of measuring the capacitance changes associated with a process vessel. Integrating the electronics has other potential benefits, as the system will be more reliable and cheaper if mass produced [5].

The ultimate aim of the work is to produce integrated electrodes with a 'footprint' that is as small as possible. This implies that, wherever possible, the electronic circuitry should be incorporated onto a custom integrated circuit. However, the spirit of the investigations to date has been to provide a flexible system that allows experimentation to find the optimum design, for instance the width of digital-analogue and analogue-digital converters can be deduced. Consequently a considerable amount of the required circuitry has been implemented using discrete integrated circuits and the resulting PCB for each electrode is 16 in². The investigations have revealed which components can be integrated and the next version will probably occupy about 5 in². One major limitation on the resulting PCB area is that the DAC for offset control needs to be 16 bits wide and therefore this should remain as a discrete chip.

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